IT IS CLAIMED:

1. A computer memory assembly, comprising:

a printed circuit host board having electronic components attached thereto forming a memory controller that is connectable with a host computer bus,

a plurality of memory cards which each have a plurality of flash EEPROM circuit chips encased therein and electrically connected to a connector along one edge thereof, and

at least one connector carried by said host board, said at least one connector being adapted to receive a connector edge of one of said memory cards and electrically connect said card to said controller.

2. The assembly according to claim 1 wherein said memory cards include:

a main circuit board including conductors attached thereto extending between said card edge connector and a plurality of rows of contacts spaced apart across a surface of said main board with a row's contacts being arranged in a predetermined pattern, and

a plurality of sub-boards each carrying more than one of said flash EEPROM integrated circuit chips and including conductors attached thereto which electrically interconnect said chips to a plurality of contacts arranged in said predetermined pattern along one edge of said sub-board, said sub-boards being attached to said main board in a manner that their edge contacts are electrically and physically attached to said rows of contacts on the main board.

3. The assembly according to either of claims 1 or 2 wherein said memory cards have an overall thickness of less than 6.0 millimeters and width along its said connector of less than 5.5 centimeters and a length of less than 9.0 centimeters.

4. The assembly according to claim 1 which additionally comprises a plurality of EEPROM integrated circuit chips carried by said host board and permanently interconnected with said memory controller.

5. The assembly according to claim 4 wherein the plurality of EEPROM integrated circuit chips carried by said host board are mounted on a plurality of sub-boards that include a plurality of contacts arranged along one edge of said sub-board, said sub-boards being attached to said host board in a manner that their edge contacts are electrically and physically attached to rows of contacts on the host board.

6. A computer memory card, comprising:

a plurality of sub-boards each carrying a plurality of flash EEPROM integrated circuit chips and including electrical conductors attached thereto which interconnect said chips to a plurality of electrical contacts along one edge of said sub-board, said contacts having a predetermined pattern therealong,

a main circuit board including electrical conductors attached thereto and extending between a plurality of electrical contacts at an edge thereof and a plurality of rows of electrical contacts on at least one side thereof that are each arranged in said pattern,

said sub-boards being attached to said main board with their edge contacts being electrically connected to respective ones of said plurality of rows of contacts on the main board, and

a cover enclosing said main printed circuit board and attached sub-boards in a manner that electrical contact may be made with said plurality of contacts at said edge of the main printed circuit board.

7. The computer memory card according to claim 6 wherein the circuit chips include a row of connection pads along one edge thereof, said sub-board contains electrical conductors insulated from said circuit chips and extending between the sub-board contacts and a plurality of contacts adjacent said circuit chips one edge, and an electrical interconnection between the circuit chip pads and said plurality of contacts adjacent thereto.

8. The computer memory card according to either of claims 6 or 7 wherein said main circuit board includes said plurality of contacts in the predetermined pattern carried on both of opposite sides thereof.

9. The computer memory card according to either of claims 6 or 7 wherein said sub-boards of memory chips are attached to said main board only through the connection of their edge contacts to respective ones of said plurality of rows of conductors on the main board.

10. The computer memory card according to either of claims 6 or 7 wherein said sub-boards of memory chips are rectangular in shape and said edge contacts are located along only one of the edges thereof that is of a longest length.

11. The assembly according to either of claims 6 or 7 wherein said memory cards have an overall thickness of less than 6.0 millimeters and width along its said connector of less than 5.5 centimeters and a length of less than 9.0 centimeters.

12. The computer memory card according to claim 6 which additionally includes a controller including at least one integrated circuit chip electrically connected between said main board edge contacts and said plurality of rows of contacts on the surface of the main board and characterized by interfacing between a host computer system bus and said memory chips.

13. The computer memory card according to claim 12 wherein said controller includes a plurality of circuit chips attached to another sub-board having electrical contacts along at least one edge which are interconnected with the conductors on said main board.

14. A computer memory card, comprising:

a plurality of memory sub-boards each carrying a plurality of flash EEPROM integrated circuit chips and including electrical conductors attached thereto which interconnect said chips to a plurality of electrical contacts along an edge of said sub-board, said contacts having a predetermined pattern therealong,

a controller sub-board carrying at least one integrated circuit chip and characterized by providing an electronic interface between a host computer system bus and said memory chips,

a main circuit board including electrical conductors attached thereto and extending between a plurality of electrical contacts at an edge thereof to said controller sub-board and to a plurality of rows of electrical contacts on a surface of said main circuit board that are each arranged in said pattern, said controller sub-board being attached to said main circuit board,

said memory sub-boards being attached to said main board with their edge contacts being electrically connected to respective ones of said plurality of rows of contacts on the main board, and

a cover enclosing said main printed circuit board and attached sub-boards in a manner that electrical contact may be made with said plurality of contacts at the edge of the main printed circuit board.

15. The computer memory card according to claim 14 wherein said main circuit board includes said plurality of rows of contacts in the predetermined pattern carried on both of opposite surfaces thereof.

16. The computer memory card according to claim 14 wherein said memory sub-boards are attached to said main board only through the connection of their edge contacts to respective ones of said plurality of rows of conductors on the main board.

17. The computer memory card according to claim 14 wherein said memory sub-boards are rectangular in shape and said edge contacts are located along only one of the edges thereof that is of a longest length.

18. In an enclosed rectangularly shaped computer memory card that is less than 5.5 centimeters in width, less than 9.0 centimeters in length and less than 6.0 millimeters in thickness, and having an electrical connector along a narrow side thereof, a combination within said card, comprising:

a main circuit board including electrical conductors carried thereby that interconnect said connector and a plurality of groups of substantially parallel rows of electrical contacts provided on opposite surfaces of said board, each of said rows having substantially the same number and spacing of contacts, and

a plurality of rectangularly shaped sub-boards each carrying a plurality of flash EEPROM integrated circuit chips electrical interconnected to a line of a plurality of electrical contacts along only one edge of said sub-board, said line having substantially the same number and spacing of contacts as does said main circuit board rows of contacts, said sub-boards being attached to said main board with their edge contacts being electrically connected to respective ones of said plurality of rows of contacts on the main board.

19. The memory card combination according to claim 18 wherein the circuit chips have contact pads provided along only one edge thereof, each of the circuit chips on a given sub-board being arranged with its contact pad edge facing the sub-board edge having the line of contacts, and wherein said sub-boards have conductors formed thereon which electrically interconnect said line of contacts to said circuit chip pads.

20. The memory card combination according to either of claims 18 or 19 wherein said sub-boards are attached to said main board only through their edge contacts being attached to said main board rows of contacts.

21. The memory card combination according to claim 18 which additionally comprises at least one integrated circuit chip carried by said main board and forming a controller to interface between a computer system bus and said memory chips, said controller chip being electrically connected in a path between said conductor and said main board rows of contacts.

22. The memory card combination according to claim 21 wherein said at least one controller chip is attached to another sub-board which in turn is mechanically and electrically attached to said main board.

23. In an enclosed rectangularly shaped computer memory system that is less than 5.5 centimeters in width, less than 9.0 centimeters in length and less than 6.0 millimeters in thickness, and having an electrical connector along one side thereof, a combination comprising a plurality of substantially identical flash EEPROM integrated circuit chips, and a controller circuit interconnected between said electrical connector and said plurality of flash EEPROM integrated circuit chips.

24. The combination of claim 23 wherein said controller circuit includes means receiving from said connector a disk memory address in the form of head, cylinder, beginning sector and sector count designations for addressing corresponding memory locations within said flash EEPROM integrated circuit chips.

25. The combination of claim 24 wherein said plurality of flash EEPROM chips are each characterized by its storage capacity being divided into physical quadrants and each quadrant having a plurality of separately addressable sectors of memory cells, wherein a chip sector includes at least a number of cells equal to a number of bits in the disk sector, and further wherein said EEPROM addressing means addresses the chips by designating an individual chip, its quadrant and a sector within that quadrant that corresponds with a disk sector address received from the connector.

26. The combination of claim 23 wherein said controller is characterized by interfacing through said connector with an industry standard IDE interface in order to translate signals received from a computer system bus according to that standard into signals that communicate with said plurality of EEPROM circuit chips.

27. In an enclosed package having an electrical connector carried thereby for interfacing with computer system signals that address disk memory by head number, cylinder number, and specific ones of a plurality of sectors that each contain a predetermined number of bytes, a mass storage system, comprising:

a plurality of flash EEPROM integrated circuit chips containing a large number of non-volatile memory cells arranged in physical quadrants on the chips and having separately addressable sectors of cells within the quadrants, the individual sectors having enough cells to store said predetermined number of bytes, and

a controller connected between said connector and said plurality of flash EEPROM integrated circuit chips in a manner to allow data to be written into said chips and to be read from said chips when a computer system is connected with said connector, said controller including means responsive to said computer address signals for addressing said plurality of EEPROM chips by corresponding chip numbers, quadrants and numbers of sectors, whereby the package of integrated circuit memory is addressed by a computer system as is disk storage memory.

28. The mass storage system according to claim 27 wherein said package is substantially rectangular in shape with a width of about 5.5 centimeters or less, a length of about 9.0 centimeters or less and a thickness of about 19 millimeters or less, and further wherein said electrical connector is mounted along one side thereof.

29. The mass storage system according to claim 27 wherein said package is a rectangularly shaped PC memory card with a width less than 5.5 centimeters,. a length less than 9.0 centimeters and a thickness of less than 6.0 millimeters, and further wherein said electrical connector is mounted along one side thereof.

30. The mass storage system according to claim 27 wherein said package has a width of about 5.4 centimeters, a length of about 7.3 centimeters and a thickness of about 19 millimeters or less, whereby said mass storage system is provided in a package that is substantially the same as an industry standard for a 1.8 inch hard disk drive.

31. The mass storage system according to claim 27 wherein said predetermined number of bytes is substantially 512.

32. The mass storage system according to claim 27 wherein said controller includes a plurality of temporary storage registers, a buffer data memory and a microprocessor, the registers and buffer memory being connected to be accessible both by a computer system through said connector and by said controller microprocessor, said microprocessor characterized by responding to a command written into one of said registers by an external computer system through the connector to carry out the command and thereafter writing into another one of said registers a status after the command has been executed.

33. The mass storage system according to claim 32 wherein said microprocessor is characterized by reading disk head, disk cylinder and disk sector addresses from others of said registers in response to a READ or a WRITE command in said one register, determining a corresponding address within the EEPROM chips, and then writing a completion status into said another one of said registers after data is read from or written into the EEPROM chip memory.

34. The mass storage system according to claim 33 wherein said microprocessor is additionally characterized by responding to a SEEK or a RESTORE command in said one register to immediately write a completion status into said another one of said registers.